What is claimed is:

		A CONTRACTOR OF THE CONTRACTOR
2		driving a terminal on the IC to a state;
3		stopping the driving of the terminal;
4		floating the terminal for a predetermined time; and
5		determining a state of the terminal after the predetermined time.
1	2.	The method of claim 1 further comprising:
2		determining quality of the IC based on the state of the terminal after the
3		predetermined time.
1	3.	The method of claim 1, wherein driving includes applying a logic low to the
2		terminal.
1	4.	The method of claim 1, wherein driving includes applying a logic high to the
2		terminal.
l	5.	The method of claim 1, wherein determining includes measuring a voltage of the
2		terminal after the predetermined time.
1	6.	A method of testing comprising:
2		charging a pin on an integrated circuit (IC) until it reaches a known state;
3		stopping the charging of the pin;
4		floating the pin for a predetermined time;
5		sampling a state of the pin after the predetermined time; and
6		determining a test result of the pin based on the state of the pin after the
7		predetermined time, wherein the method is performed with Boundary
8		Scan.

- The method of claim 6, wherein charging includes driving the pin to a logic low.
- 1 8. The method of claim 6, wherein charging includes driving the pin to a logic high.
- 1 9. The method of claim 6, wherein sampling includes determining if the pin changes state after the predetermined time.
- 1 18. A method of testing comprising:

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- driving the first terminal on an integrated circuit (IC) to a first state;
- driving the second terminal on the IC to a second state;
- 4 stopping the driving of at least one of the terminals;
- floating at least one of the terminals for a predetermined time; and
- 6 determining a state of at least one of the terminals after the predetermined
- 1 11. The method of claim 10 further comprising:
- 2 determining quality of the IC based on the state of at least one of the terminal after
- 3 the predetermined time.

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- 1 12. The method of claim 10, wherein driving the first and second terminals include
- 2 applying opposite states to the terminals.
- 1 13. The method of claim 10, wherein determining includes measuring a voltage value
- 2 of least one of the terminals.

1	Ŋ.	A method of testing comprising:
2	,	charging the first pin on an integrated circuit (IC) to a first known state;
3		charging the second pin on the IC to a second known state;
4		stopping the charging of at least one of the pins;
5		floating at least one of the pins for a predetermined time;
6		sampling a state of at least one of the pins after the predetermined time; and
7		determining a test result of at least one of the pins based on the state of at least
8		one the pins after the predetermined time, wherein the method is
9		performed with Boundary Scan.
1	15.	The method of claim 14, wherein charging the first and second terminals includes
2		applying opposite states to the terminals.
1	16.	The method of claim 14, wherein sampling includes determining whether at least
2		one of the pin changes state after the predetermined time.
1	17.	A method of testing a circuit module, the method comprising:
2		tri-stating all of the terminals on any of the integrated circuits (ICs) connected
3		to a net, the ICs located on the same circuit module, and wherein the ICs
4		includes different types of ICs and perform different functions,
5		driving the net to a state through a terminal on one or more of the ICs;
6		stopping the driving of the terminal;
7		floating the net for a predetermined time; and
8		determining a state of the net after the predetermined time, wherein the
9		method is performed with Boundary Scan.
1	18.	The method of claim 17 further includes:
2		determining quality of the circuit module based on the state of the net after the
3		predetermined time.

1	19.	The method of claim 17, wherein determining includes determining if the net
2	,	changes from one state to another.
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1	20.	An apparatus comprising:
2		an integrated circuit (IC); and
3		a tester connected to the IC, wherein the tester performs leakage test on the IC by
4		a method of:
5		driving the terminal of an IC to a state;
6		stopping the driving of the terminal;
7		floating the terminal for a predetermined time; and
8		determining a state of the terminal after the predetermined time.
1	21.	The apparatus of claim 20, wherein the IC includes a plurality of Boundary Scan
2		pins, wherein the tester connects to the IC through the Boundary Scan pins.
1	22.	The apparatus of claim 20, wherein the tester is a computer.
1	23.	An apparatus comprising:
2		an integrated circuit (IC); and
3		a tester connected to the IC, wherein the tester performs a leakage test on the IC
4		by a method of:
5		driving the first terminal of an IC to a first state;
6		driving the second terminal of an IC to a second state;
7		stopping the driving of at least one of the terminals;
8		floating at least one of the terminals for a predetermined time; and
9		determining a state of at least one of the terminals after the predetermined
10		time, wherein the method is performed with Boundary Scan.
1	24.	The apparatus of claim 23, wherein the IC comprises a plurality of Boundary Scar
2		pins, wherein the tester connects to the IC through the Boundary Scan pins.
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- 1 25. The apparatus of claim 23, wherein the tester performs the leakage test through
- 2 \ \ \ the Boundary Scan pins.
- 1 26. The apparatus of claim 23, wherein the tester is a computer.
- 1 27. A machine-readable medium having instructions stored thereon capable of
- 2 causing a tester to perform method of testing, the method comprising:
- 3 charging the pin of an integrated circuit (IC) until it reaches a known state;
- 4 stopping the charging of the pin;
- 5 floating the pin for a predetermined time;
- 6 sampling a state of the pin after the predetermined time; and
- determining a test result of the pin based on the state of the pin after the
- 8 predetermined time.
- 1 28. The method of claim 27, wherein charging includes driving the pin to a logic low.
- 1 29. The method of claim 27, wherein charging includes driving the pin to a logic
- 2 high.
- 1 30. The method of claim 27, wherein sampling includes determining if the pin
- 2 changes state after the predetermined time.